REMARKS

This is a full and timely response to the non-final Office Action mailed May 11, 2007. Upon entry of the foregoing amendments, claims 2-7 and 12-26 are pending in the application. Claims 2, 7, 12 and 19 have been amended. Claims 1 and 8-11 were previously canceled. The subject matter of amended claims 2, 7, 12 and 19 can be found in the originally filed specification in at least FIGs. 7 and 9 and the related detailed description. Consequently, no new matter is added to the present application. In light of the foregoing amendments and following remarks, Applicants request reconsideration of the application and pending claims.

I. Claim Rejections Under 35 USC § 112 – Claims 2 and 7

A. Statement of the Rejection

Claims 2 and 7 stand rejected under 35 USC § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter that applicant regards as the invention. Specifically, concerning claim 2, the Office Action alleges that there is insufficient antecedent basis for the limitation "the I/O pin" in lines 5 and 8 of the claim. Regarding claim 7, the Office Action alleges that there is insufficient antecedent basis for the limitation "the first I/O pin" in lines 3 and 5.

B. Discussion of the Rejection

Applicants have amended claim 2 and claim 7. Specifically, claim 2, as amended, includes "an input output (I/O) pin" in line 3. Thus, the limitation "the I/O pin" on lines 4 and 6 has sufficient antecedent basis. Claim 7, as amended, includes "the I/O pin." Claim 7 depends from independent claim 2. Thus, claim 7, as amended includes sufficient antecedent basis for the limitation "the I/O pin." Accordingly, Applicants respectfully request that the rejection of claims 2 and 7 under 35 USC § 112, second paragraph, be withdrawn.

II. Claim Rejections Under 35 USC § 103 – Claims 2-7 and 12-26

A. Statement of the Rejections

Claims 2, 5-7 and 12-26 stand rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Applicants admitted prior art (AAPA) in view of U.S. Patent No. 6,833,728 to Chennupati, hereafter *Chennupati*.

Claims 3 and 4 stand rejected under 35 U.S.C. § 103(a) as allegedly being obvious over AAPA and *Chennupati* in view of U.S. Patent No. 6,271,732 to Herzel, hereafter *Herzel*.

B. Discussion of the Rejections

A *prima facie* case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art. *In re Rinehart,* 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Applicants' independent claims 2, 12 and 19, as amended, comprise respective features that are not disclosed, taught, or suggested by the prior art.

1. Claims 2 and 5-7

Applicants' independent claim 2, as amended, is directed to an integrated circuit that comprises "an input/output (I/O) pin coupled to the input and the output of the scan path, wherein the I/O pin inputs scan test data to the scan path at a first test time responsive to an input enable control signal."

In contrast with Applicants' claimed integrated circuit, the proposed combination of AAPA in view of *Chennupati* does not disclose, teach or suggest an

I/O pin that inputs scan test data to the scan path at a first test time responsive to an input enable control signal. Applicants' AAPA (FIGs. 1-4) does not disclose, teach or suggest an I/O pin responsive to an input enable control signal.

Applicants' FIG. 1 shows separate input and output pins. Specifically, an input pin 2 is coupled to input logic 3. An output pin 12 is coupled to output logic 11. FIG. 1 is devoid of a control signal of any kind.

Applicants' FIG. 2 shows a compactor 9 that receives scan chain output data from N scan chains 10. The compactor 9 contains a number of serially connected cyclic shift register cells (CSRCs) that form a cyclic shift register. Scan input data signals (SID) applied to the scan chains 10 are forwarded with internally generated compactor feedback data (CFD) signals from the cyclic shift register cells to XOR gates 11. When all the scan output data has been shifted through the cyclic shift register 12, the value retained can be shifted out and analyzed as a compacted output data (COD) signal. FIG. 2 is devoid of a control signal.

Applicants' FIG. 3 shows a circuit that includes an AND gate 15 and a flip-flop 17. The AND gate 15 receives scan output data 8 and a mask signal 13. The mask signal 13 determines when a data signal is provided from the AND gate 15 to the flip-flop 17. Consequently, one can mask the scan output data for a desired clock cycle. A mask signal 13 that determines when scan data 8 is applied to a flip-flop 17 does not disclose, teach or suggest an I/O pin of an integrated circuit that inputs scan test data to a scan path responsive to an input enable control signal.

Applicants' FIG. 4 shows a circuit for seeding or initializing a built-in self test. The circuit includes multiplexer 22, multiplexer 25, XOR gate 29 and flip-flop 20. The circuit has four inputs and an output. The XOR gate 29 receives a first signal 27 from a linear feedback shift register and scan output data 28. The output of XOR gate 29 is coupled to a first input of multiplexer 25. A second input of multiplexer 25 is coupled to an output of multiplexer 22. The output of multiplexer 25 is coupled to flip-flop 20. The flip-flop 20 generates a feedback signal 26 that is responsive to a clock input and the output of multiplexer 25. The multiplexer 22 receives a seed value via input 21 and the feedback signal 26 and forwards scan input data 23 to multiplexer 25 and one or more other destinations (not shown). While each of the seed value 21, clock, and linear feedback shift register 27 signals can be interpreted as

control signals, neither of these signals is responsible for directing an I/O pin to input scan test data to a scan path at a first test time, as required by Applicants' claimed integrated circuit.

Chennupati fails to remedy the failure of AAPA to disclose, teach or suggest Applicants' claimed integrated circuit. *Chennupati* shows a system for simultaneous bi-directional signal transmission over a transmission line. Each of the I/O pins shown in *Chennupati* are coupled to a bridge (110, 158) and an input arithmetic unit (116, 164). The bridge 110 has a first terminal 112 and a second terminal 114. The first terminal 112 is coupled to driver 106 and second terminal 114 is coupled to interface port 104 (i.e., an I/O pin). The bridge 110 has a resistance of Ra1. The bridge 110 may be a resistor having two ends connected to first terminal 112 and to second terminal 114, respectively. In accordance with column 4, lines 60-61, the operation of device 150 is similar to that of device 102. Thus, *Chennupati* is devoid of any further connection to the I/O pins.

As shown above, the proposed combination of AAPA and *Chennupati* is entirely silent regarding "an input/output (I/O) pin coupled to the input and the output of the scan path, wherein the I/O pin inputs scan test data to the scan path at a first test time responsive to an input enable control signal." Accordingly, the proposed combination fails to establish a *prima facie* case of obviousness as to Applicants' amended independent claim 2 and the rejection of claim 2 under 35 U.S.C. § 103(a) should be withdrawn.

For at least the reason that claims 5-7 depend directly from claim 2 and include all the features of independent claim 2, the rejection of claims 5-7 under 35 U.S.C. § 103(a) should also be withdrawn. *In re Fine,* 837 F.2d 1071, 5 USPQ 2d 1596, 1598 (Fed. Cir. 1998).

2. Claims 12-18

Applicants' independent claim 12, as amended, is directed to an integrated circuit that includes I/O circuitry that comprises "an input buffer responsive to an input enable control signal and coupled to (1) the I/O pin," and "a virtual pin output buffer responsive to a virtual pin enable control signal," among other features.

In contrast with Applicants' claimed integrated circuit, the proposed combination of AAPA in view of *Chennupati* does not disclose, teach or suggest an input buffer responsive to an input enable control signal coupled to the I/O pin and a virtual pin output buffer responsive to a virtual pin enable control signal. As shown above, Applicants' AAPA (FIGs. 1-4) does not disclose, teach or suggest an I/O pin responsive to an input enable control signal. Furthermore, Applicants' AAPA does not disclose, teach or suggest a virtual pin output buffer responsive to a virtual pin enable control signal.

Applicants' FIGs. 1 and 2 are devoid of a control signal of any kind.

Applicants' FIG. 3 shows a mask signal 13 that determines when a data signal is provided from the AND gate 15 to the flip-flop 17. Consequently, one can mask the scan output data for a desired clock cycle. A mask signal 13 that determines when scan data 8 is applied to a flip-flop 17 does not disclose, teach or suggest an I/O pin of an integrated circuit that inputs scan test data to a scan path responsive to an input enable control signal. Moreover, the prior art mask signal does not disclose, teach or suggest a virtual pin output buffer responsive to a virtual pin enable control signal.

Applicants' FIG. 4 shows a circuit with a seed value 21, clock, and linear feedback shift register 27 input signals for seeding or initializing a built-in self test. While each of the seed value 21, clock, and linear feedback shift register 27 signals can be interpreted as control signals, neither of these signals is responsible for directing an I/O pin to input scan test data to a scan path at a first test time, as required by Applicants' claimed integrated circuit. Moreover, the prior art seed value 21, clock, and linear feedback shift register 27 signals for seeding or initializing a built-in self test do not disclose, teach or suggest a virtual pin output buffer responsive to a virtual pin enable control signal.

Chennupati fails to remedy the failure of AAPA to disclose, teach or suggest Applicants' claimed integrated circuit. *Chennupati* shows a system for simultaneous bi-directional signal transmission over a transmission line. Each of the I/O pins shown in *Chennupati* are coupled to a bridge (110, 158) and an input arithmetic unit (116, 164). The bridge 110 has a first terminal 112 and a second terminal 114. The first terminal 112 is coupled to driver 106 and second terminal 114 is coupled to interface port 104 (i.e., an I/O pin). The bridge 110 has a resistance of Ra1. The

bridge 110 may be a resistor having two ends connected to first terminal 112 and to second terminal 114, respectively. In accordance with column 4, lines 60-61, the operation of device 150 is similar to that of device 102. *Chennupati* is devoid of any further connection to the I/O pins.

Accordingly, the proposed combination of AAPA and *Chennupati* is entirely silent regarding an input buffer responsive to an input enable control signal coupled to the I/O pin and a virtual pin output buffer responsive to a virtual pin enable control signal. Accordingly, the proposed combination fails to establish a *prima facie* case of obviousness as to Applicants' amended independent claim 12 and the rejection of claim 12 under 35 U.S.C. § 103(a) should be withdrawn.

For at least the reason that claims 13-18 depend directly or indirectly from claim 12 and include all the features of independent claim 12, the rejection of claims 13-18 under 35 U.S.C. § 103(a) should also be withdrawn. *See In re Fine, supra.*

3. Claims 19-26

Applicants' independent claim 19, as amended, is directed to a method that includes the steps of "processing the scan data in a respective scan path to produce scan output data in response to an input enable control signal and a mode control signal," and "outputting scan output data to the I/O pin at a second time in response to an output enable control signal."

In contrast with Applicants' claimed method, the proposed combination of AAPA in view of *Chennupati* does not disclose, teach or suggest processing the scan data in a respective scan path to produce scan output data in response to an input enable control signal and a mode control signal and outputting scan output data to the I/O pin at a second time in response to an output enable control signal. As shown above, Applicants' AAPA (FIGs. 1-4) does not disclose, teach or suggest an I/O pin responsive to an input enable control signal. Furthermore, Applicants' AAPA does not disclose, teach or suggest processing scan data in response to a mode control signal. Moreover, Applicants' AAPA does not disclose, teach or suggest outputting scan output data to the I/O pin at a second time in response to an output enable control signal.

Applicants' FIGs. 1 and 2 are devoid of a control signal of any kind.

Applicants' FIG. 3 shows a mask signal 13 that determines when a data signal is provided from the AND gate 15 to the flip-flop 17. Consequently, one can mask the scan output data for a desired clock cycle. A mask signal 13 that determines when scan data 8 is applied to a flip-flop 17 does not disclose, teach or suggest an I/O pin of an integrated circuit that inputs scan test data to a scan path responsive to an input enable control signal and a mode control signal Moreover, the prior art mask signal does not disclose, teach or suggest outputting scan output data to the I/O pin at a second time in response to an output enable control signal.

Applicants' FIG. 4 shows a circuit with a seed value 21, clock, and linear feedback shift register 27 input signals for seeding or initializing a built-in self test. While each of the seed value 21, clock, and linear feedback shift register 27 signals can be interpreted as control signals, neither of these signals is responsible for directing an I/O pin to input scan test data to a scan path at a first test time, as required by Applicants' claimed method. Moreover, the prior art seed value 21, clock, and linear feedback shift register 27 signals for seeding or initializing a built-in self test do not disclose, teach or suggest outputting scan output data to the I/O pin at a second time in response to an output enable control signal.

Chennupati fails to remedy the failure of AAPA to disclose, teach or suggest Applicants' claimed method. *Chennupati* shows a system for simultaneous bi-directional signal transmission over a transmission line. Each of the I/O pins shown in *Chennupati* are coupled to a bridge (110, 158) and an input arithmetic unit (116, 164). The bridge 110 has a first terminal 112 and a second terminal 114. The first terminal 112 is coupled to driver 106 and second terminal 114 is coupled to interface port 104 (i.e., an I/O pin). The bridge 110 has a resistance of Ra1. The bridge 110 may be a resistor having two ends connected to first terminal 112 and to second terminal 114, respectively. In accordance with column 4, lines 60-61, the operation of device 150 is similar to that of device 102. *Chennupati* is devoid of any further connection to the I/O pins.

Accordingly, the proposed combination of AAPA and *Chennupati* is entirely silent regarding "processing the scan data in a respective scan path to produce scan output data in response to an input enable control signal and a mode control signal," and "outputting scan output data to the I/O pin at a second time in response to an

output enable control signal." Consequently, the proposed combination fails to establish a *prima facie* case of obviousness as to Applicants' amended independent claim 19 and the rejection of claim 19 under 35 U.S.C. § 103(a) should be withdrawn.

For at least the reason that claims 20-26 depend directly or indirectly from claim 19 and include all the features of independent claim 19, the rejection of claims 20-26 under 35 U.S.C. § 103(a) should also be withdrawn. *See In re Fine, supra.*

4. Claims 3 and 4

Applicants' independent claim 2, as amended, is directed to an integrated circuit that comprises "an input/output (I/O) pin coupled to the input and the output of the scan path, wherein the I/O pin inputs scan test data to the scan path at a first test time responsive to an input enable control signal."

In contrast with Applicants' claimed integrated circuit, the proposed combination of AAPA and *Chennupati* in view of *Herzel* does not disclose, teach or suggest an I/O pin that inputs scan test data to the scan path at a first test time responsive to an input enable control signal.

In contrast with Applicants' claimed integrated circuit, the proposed combination does not disclose, teach or suggest an input buffer responsive to an input enable control signal coupled to the I/O pin and a virtual pin output buffer responsive to a virtual pin enable control signal. As shown above, Applicants' AAPA (FIGs. 1-4) does not disclose, teach or suggest an I/O pin responsive to an input enable control signal. As further shown above, *Chennupati* fails to remedy the failure of AAPA to disclose, teach or suggest Applicants' claimed integrated circuit. *Chennupati* shows a resistor bridge and an arithmetic unit coupled to each of the I/O pins. *Chennupati* is devoid of any further connection to the I/O pins. *Herzel* fails to remedy the failure of AAPA and *Chennupati* to disclose, teach or suggest each feature of Applicants' claimed integrated circuit. *Herzel* shows a ring oscillator consisting of series connected amplifier stages that are alternatively energized by first and second voltages that are negatively correlated to each other. *See Herzel Abstract*.

Accordingly, the proposed combination is entirely silent regarding "an input/output (I/O) pin coupled to the input and the output of the scan path, wherein the I/O pin inputs scan test data to the scan path at a first test time responsive to an

input enable control signal." Accordingly, the proposed combination fails to establish a *prima facie* case of obviousness as to Applicants' dependent claims 3 and 4 and the rejection of these claims under 35 U.S.C. § 103(a) should be withdrawn.

CONCLUSION

For at least the reasons set forth above, Applicants respectfully submit that pending claims 2-7 and 12-26 are allowable over the cited art of record and the present application is in condition for allowance. Accordingly, a Notice of Allowance is respectfully solicited. Should the Examiner have any comments regarding the Applicants' response, Applicants request that the Examiner telephone Applicants' undersigned attorney.

Respectfully submitted,

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